Electronic Version

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Claims

[c1] 1.A method of determining critical areas associated with different types of fault mechanisms in an integrated circuit design, said method comprising:
constructing individual Voronoi diagrams for critical areas of individual fault mechanisms;
constructing a composite Voronoi diagram based on said individual Voronoi diagrams; and
computing the critical area for composite fault mechanisms of said integrated circuit design based on said composite Voronoi diagram.

[c2] 2.The method in claim 1, wherein said constructing of said composite Voronoi diagram comprises a mapping of minimum values of said individual Voronoi diagrams.

[c3] 3.The method in claim 1, wherein said constructing of said composite Voronoi diagram comprises a mapping of maximum values of said individual Voronoi diagrams.

[c4] 4.The method in claim 1, wherein said constructing of said composite Voronoi diagram comprises constructing a three dimensional representation of critical area for said composite fault mechanism.

[c5] 5.The method in claim 1, wherein said constructing of said composite Voronoi diagram comprises forming a logical OR composite of said individual fault mechanisms.

[c6] 6. The method in claim 1, wherein said constructing of said composite Voronoi diagram comprises forming a logical AND composite of said individual fault mechanisms.

[c7] 7.The method in claim 1, wherein said constructing of said composite Voronoi diagram comprises forming a logical NOT of said individual fault mechanisms.

[c8] 8.A method of determining critical areas associated with different types of fault mechanisms in an integrated circuit design, said method comprising:
constructing individual Voronoi diagrams for critical areas of individual fault mechanisms;
constructing a logical OR composite Voronoi diagram of said individual Voronoi diagrams; and
computing the critical area for composite fault mechanisms of said integrated circuit design based on said composite Voronoi diagram.

[c9] 9.The method in claim 8, wherein said constructing of said composite Voronoi diagram comprises a mapping of

minimum values of component individual Voronoi diagrams.

[c10] 10.The method in claim 8, wherein said constructing of said composite Voronoi diagram comprises constructing a three dimensional representation of critical area for said composite fault mechanism.

[c11] 11. The method in claim 8, further comprising computing the critical area of a logical NOT of said individual fault mechanisms in a process comprising subtracting the critical area of said individual fault mechanisms from the area of said integrated circuit.

[c12] 12.The method in claim 8, further comprising computing the critical area of a logical AND of said individual fault mechanisms in a process comprising:
adding the critical areas of a first individual fault mechanism to a second individual fault mechanism to produce an intermediate result; and
subtracting the critical area of said logical OR composite of said first individual fault mechanism and said second individual fault mechanism from said intermediate result.

[c13] 13.The method in claim 8, further comprising computing the critical area of any boolean composition of said individual fault mechanisms in a process comprising:

arranging the boolean composition into disjunctive normal form; and
computing the sums and differences of component critical areas of logical OR composites of subsets of said individual fault mechanisms.

[c14] 14.The method in claim 8, further comprising computing the critical area of any boolean composition of said fault individual mechanisms in a process comprising:
arranging the boolean composition into conjunctive normal form;
computing the sums and differences of component critical areas of logical OR composites of subsets of said individual fault mechanisms to obtain an intermediate result; and
subtracting said intermediate result from the area of said integrated circuit.

[c15] 15.A program storage device readable by machine, tangibly embodying a program of instructions executable by the machine to perform a method of determining critical areas associated with different types of fault mechanisms in an integrated circuit design, said method comprising:
constructing individual Voronoi diagrams for critical areas of individual fault mechanisms;
constructing a composite Voronoi diagram based on said

individual Voronoi diagrams; and

computing the critical area for composite fault mechanisms of said integrated circuit design based on said composite Voronoi diagram.

[c16] 16.The program storage device in claim 15, wherein said constructing of said composite Voronoi diagram comprises a mapping of minimum values of said individual Voronoi diagrams.

[c17] 17.The program storage device in claim 15, wherein said constructing of said composite Voronoi diagram comprises a mapping of maximum values of said individual Voronoi diagrams.

[c18] 18.The program storage device in claim 15, wherein said constructing of said composite Voronoi diagram comprises constructing a three dimensional representation of critical area for said composite fault mechanism.

[c19] 19.The program storage device in claim 15, wherein said constructing of said composite Voronoi diagram comprises forming a logical OR composite of said individual fault mechanisms.

[c20] 20. The program storage device in claim 15, wherein said constructing of said composite Voronoi diagram comprises forming a logical AND composite of said indi-

vidual fault mechanisms.